

**REMARKS**

Claims 1-14 are pending in the application. By this amendment, claims 2 and 10 are being cancelled.

Claims 1-4, 9 and 10 have been rejected under 35 USC 102(e) as being anticipated by Whitton (US6172964). The rejection is respectfully traversed.

Whitton discloses a clock synchronization mechanism. A network interface for an asynchronous cell switched communication network includes a data input, a memory for buffering data received at the data input, and a clock signal generator for providing a clock signal having a frequency which is controlled in accordance with a fill level of the buffer memory. The clock signal is used to control a rate of transfer of data from the buffer memory. Data received at the network interface device is consumed by a FIFO buffer. When the buffer fill level exceeds a predetermined level, the clock signal frequency is increased and conversely, when the buffer fill level drops below the predetermined level, the clock signal frequency is decreased. (Abstract)

The predetermined level in Whitton appears to be an equilibrium fill level, though Whitton also indicates that at equilibrium the fill level will vary between a known upper and lower limit determined by the amount of cell delay variation. (col. 3, lines 3-4; 45-47.) Further, Whitton's claim 1 refers to increasing the clock frequency when a buffer memory fill level exceeds the predetermined level and decreasing the clock frequency when the buffer memory fill level drops below that same predetermined level. In any case, the adjustment mechanism for Whitton includes loading a count value into a counter controlled by a local clock source to generate the clock reference, the count value being varied in accordance with the buffer memory fill level.

In contrast, the present invention does not simply divide the local oscillator signal by a decremented or incremented divisor to speed up or slow down the clock, respectively. Rather, the present invention is based in part on avoiding abrupt changes in the clock reference frequency so as not to adversely affect voice quality. This is achieved by the introduction of a half-cycle clock stretch to gain the proper clock adjustment. In particular, the reference clock is stretched by half a cycle of the oscillator clock. (See specification at page 17, line 16 to page 18, line 2.) Thus, with a buffer fullness between a high and low threshold, the present approach a nominal clock rate is used (no clock stretch and a nominal divisor, e.g., 4096). When buffer fullness

exceeds the high threshold, a fast clock is chosen (clock stretch and decremented divisor, e.g., 4095). When the buffer fullness drops below the low threshold, a slow clock is used (clock stretch and nominal divisor, e.g., 4096).

Whitton simply adjusts a counter value up or down to affect the clock frequency. There is no teaching or suggestion in Whitton regarding use of clock stretching as recited in amended claim 1: “upon buffer fullness exceeding a high buffer threshold, adjusting the clock reference frequency upwards by setting the clock divisor to a value less than the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal; upon buffer fullness dropping below a low buffer threshold, adjusting the clock reference frequency downwards by setting the clock divisor to the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal.” Thus, Whitton cannot anticipate claim 1 as amended. Claim 9 has been amended in a similar manner. Dependent claims 3 and 4 have been amended to further clarify the manner of clock adjustment. As these claims depend from claim 1, the remarks above for claim 1 as amended apply. Reconsideration of the rejection under 35 USC 102(e) is respectfully requested.

Claims 7, 8, 13 and 14 have been rejected under 35 USC 103(a) as being unpatentable over Whitton in view of Bernstein (US5912880). Claims 5, 6, 11 and 12 have been rejected under 35 USC 103(a) as being unpatentable over Whitton in view of Bernstein and Lauret (US6252850).

Dependent claims 5-8 and 11-14 depend from rejected base claims 1 and 9, respectively. Claims 5-8 and 11-14 are patentable for reasons noted above with respect to amended claims 1 and 9, respectively.

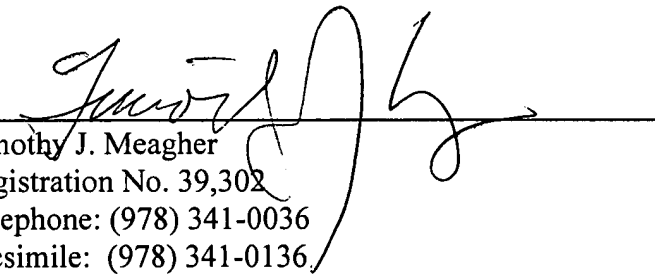
**CONCLUSION**

In view of the above amendments and remarks, it is believed that all pending claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By

  
Timothy J. Meagher  
Registration No. 39,302  
Telephone: (978) 341-0036  
Facsimile: (978) 341-0136

Concord, MA 01742-9133

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